ABSTRACT

A valve control system for a semiconductor processing chamber includes a system control computer and a plurality of electrically controlled valves associated with the processing chamber. The system further includes a programmable logic controller in communication with the system control computer and operatively coupled to the electrically controlled valves. The refresh time for control of the valves may be less than 10 milliseconds. Consequently, valve control operations do not significantly extend the period of time required for highly repetitive cycling in atomic layer deposition processes. A hardware interlock may be implemented through the output power supply of the programmable logic controller.